Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore

Name of Program: Bachelor of Technology in Electronics & Communication

SUBJECT CODE	Category	SUBJECT NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		Th	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
BTEC501	EC	**Microprocessors & Interfacing**	60	20	20	30	20	3	1	2	5

Legends: **Th** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical; **C** - Credit;
***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Educational Objectives (CEOs):

To provide a theoretical & practical knowledge of Microprocessor architecture, interfacing and assembly language programming techniques.

Course Outcomes (COs):

After completion of this course the students are expected to be able to demonstrate following knowledge, skills and attitudes

The students will be able to

1. Demonstrate knowledge of the architecture, organization and operation of microprocessors (8085 and 8086), peripherals and memories typically interfaced with microprocessors.
2. Execute assembly language programs efficiently for solving problems by using instruction sets of microprocessor.
3. Use an Integrated Development Environment (IDE) as a modern software tool for microprocessor and embedded systems development. (Application &Synthesis).

Syllabus

Unit-I
8085 Microprocessor Architecture and Interfacing

Introduction to microprocessor, 8085 microprocessor, 8085 Pin Functions, Architecture, Register Set, Flag Classification, ALU and control & timing unit, Memory Interfacing, Interfacing Input Output Devices, Memory-Mapped I/O. Timing diagram for I/O and memory read/write cycle.

Unit-II
Addressing Modes and Instruction set

Addressing Modes of 8085 Microprocessor, Instruction Format, Opcode and operand, Classification of Instructions: Data transfer, Arithmetic, Logical, Rotate, Branch and machine Control instructions.

Development of 8085 assembly language programs. Concept of stack and Instruction related to stack. 8085 interrupts, RST, RIM, SIM instructions. Subroutines and conditional call instruction. Counter and Time Delay Programs.

Unit-III
Introduction of 8086 Microprocessor

Architecture of 8086 Microprocessor, BIU and EU, pin diagram, register organization, memory organization, Segments, maximum and minimum modes, Interrupts of 8086.

Unit-IV
Addressing Modes and ALP

Instruction formats, addressing modes, 8086 assembly language programming using Instruction set of 8086 Microprocessor: data transfer instructions, arithmetic instructions, branch instructions, looping instructions, NOP and HLT instructions, flag manipulation instructions, logical instructions shift and rotate instructions.

Unit-V
Peripheral devices and Interfacing

Programmable input/output ports 8255A: Configuration, Modes and Operation. Programmable interval timer 8253, keyboard/display controller 8279, Programmable communication interface 8251 USART, DMA controller 8257.

Text Books:

1. Ramesh S. Gaonkar, "Microprocessor Architecture, Programming and application with 8085", 6th Edition, Penram International Publishing, 2013.
2. B. Ram, "Fundamentals of Microprocessors and Microcontrollers", 6th Edition, Dhanpat Rai Publications, 2010.
3. Douglas V. Hall, "Microprocessors and Interfacing: Programming and Hardware", 3rd Edition, Tata McGraw Hill Publishers, 2012.

References Books:

1. A. K. Ray and K. M. Burchandi, "Intel Microprocessors Architecture Programming and Interfacing", 3rd Edition, McGraw Hill International Edition, 2012.
2. Barry B. Brey, "The Intel Microprocessors – Architecture, Programming And Interfacing", 8th Edition, Pearson Education, 2008.
3. Adithya P Mathur, "Introduction to Microprocessor", 3rd Edition, Tata McGraw Hill Publishers, 2001.
4. John Uffenbeck, "The 80x86 Families, Design, Programming and Interfacing", 3rd Edition, Pearson Education, 2002.

List of Experiments:

Develop/Execute a program:-

1. To move data from one register to another.
2. To move immediate data between different registers.
3. For addition and subtraction.

4. For multiplication.
5. For division.
6. To check whether given no is odd or even.
7. To transfer a block of data from one memory location to another memory location.
8. To add two 32-bit numbers.
9. To add 2 decimal numbers in BCD format.
10. To convert data from gray code to binary code.
11. To convert data from binary code to gray code.
12. Based on 8 bit Logical instructions.
13. To sum integers from 0 to 9.
14. To count negative values in given block of data.
15. To find the smallest number from an array of N numbers.
16. Develop/Execute a Subroutine to find the square of given integer.

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SUB-JECT CODE	Cate-gory	SUBJECT NAME	TEACHING &EVALUATION SCHEME								
			THEORY			PRACTICAL		T h	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
BTEC502	EC	Cellular & Mobile Communication	60	20	20	0	0	3	1	0	4

Legends: **L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical; **C** - Credit;
***Teacher Assessment** shall be based following components: Quiz/Assignment/Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Educational Objectives (CEOs):

The subject aims to provide the student with:

1. To impart fundamental concepts in cellular technology, models of mobile radio channels, communication technologies adapted and wireless networks.
2. Be acquainted with different interference factors influencing cellular and mobile communications.
3. To efficiently use the background behind developing different path loss and/or radio coverage in cellular environment.
4. To expose the students to the most recent technological developments in mobile communication systems.

Course Outcomes (COs):

1. Students will get familiar with cellular terminology as mobile station, base station and mobile telephone switching office.
2. Develop the capability to analyze and design propagation models for mobile radio channel.
3. Learn how to reduce co-channel and non co-channel interference.
4. Know about implementation of digital cellular system.

Syllabus

UNIT-I

Introduction To Cellular Mobile Systems: Limitations of Conventional Mobile Telephone System, Basic Cellular Systems, Performance Criteria, Uniqueness of Mobile Radio Environment, Operation of Cellular Systems, Analog & Digital Cellular Systems.

UNIT-II

Cellular Concept: Concept of Frequency Reuse, Co-channel Interference Reduction Factor, Desired C/I in An Omni-directional Antenna System, Sectoring and Cell Splitting, System Capacity, Trunking and Grade of Service (GOS), Concept of Handoff, Types of Handoff, Queuing of Handoff

UNIT-III

Cell Coverage for Signal and Traffic : Signal Reflections in Flat and Hilly Terrain, Effect of Human Made Structures, Phase Difference between Direct and Reflected Paths, Straight Line Path Loss Slope, General Formula for Mobile Propagation Between Two Fixed Station Over Water and Flat Open Area, Near- in and Long Distance Propagation. Mobile to Mobile Propagation.

UNIT-IV

Interference in Cellular Mobile System: Co-channel Interference: Design of an Omni-directional Antenna System and Directional Antenna System, Lowering the Antenna Height, Power Control, Reduction in C/I by Tilting Antenna, Umbrella Pattern Effect. Non Co-channel Interference: Adjacent-Channel Interference, Next Channel Interference and Neighboring Channel Interference, Near-End Far-End Interference, Diversity Receiver

Frequency Management, Channel Assignment: Frequency Management, Frequency-Spectrum Utilization, Set-up Channels, Fixed Channel Assignment Schemes, Dynamic Channel Assignment Schemes,

UNIT-V

Digital Cellular System: Multiple Access Techniques – FDMA/FDD, TDMA/TDD, CDMA, SDMA and OFDMA/SC-FDMA/SOFDMA/MIMO, GSM System Architecture, GSM Radio Subsystem, GSM Channel Types, Frame Structure for GSM, Signal Processing in GSM, GPRS and EDGE.

TEXT BOOKS:

1. William C. Y. Lee, Mobile Cellular Telecommunications: Analog and Digital Systems, 2nd Edition, Tata McGraw Hill Publication, 1995.
2. Theodore S. Rappaport, Wireless Communications: Principles and Practice, 2nd Edition, Pearson / PHI Publication, 1996.

REFERENCES:

1. Iti Saha Misra, Wireless Communications and Networks: 3G and Beyond, 2nd Edition, Tata McGraw Hill Publication, 2013.
2. Gordon L. Stuber, Principles of Mobile Communications, Springer International 2nd Edition, 2007.
3. William Stallings, "Wireless Communications and Networks", 2nd Edition, Pearson Education, 2005.
4. Siegmund M. Redl, Mathias K. Weber, Malcolm W. Oliphant, "An Introduction to GSM", Artech House Publishers, 1998.

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SUBJECT CODE	Category	SUBJECT NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		Th	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
BTEC503	EC	Digital Communication	60	20	20	30	20	3	1	2	5

Legends: **Th** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical; **C** - Credit; ***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Educational Objectives (CEOs):

1. Understand basic components of digital communication systems.
2. Design optimum receivers for digital modulation techniques.
3. Analyze the error performance of digital modulation techniques.
4. Design digital communication systems under given power, spectral and error performance constrains.

Course Outcomes (COs):

After successfully completing the course students will be able to

1. Define Sampling theorem and explain the various aspects of sampling theorem viz. Aliasing, signal distortion.
2. Identify and explain the techniques used for waveform coding viz. Pulse Amplitude Modulation (PAM) and Pulse Code Modulation (PCM).
3. Describe different digital modulation schemes, and compare advantages and disadvantages of each as applied to baseband signal.

Unit I

Introduction to Sampling, Spectrum of Sampled Signal, Aliasing, Nyquist Criterion, Signal Reconstruction from Sampled Signal, Pulse Amplitude Modulation, Quantization, Uniform Quantizers: Midrise and Midtread, Quantization noise, Lloyd Max Quantization Algorithm, Pulse Code Modulation, Non uniform Quantizers, Delta Modulation, Differential Pulse Code Modulation (DPCM).

Unit II

Cumulative distribution function, Probability density function, Mean, Variance and standard deviations of random variable, Gaussian distribution, Error function, Correlation and autocorrelation, Central-limit theorem, Error probability, Power Spectral density of digital data.

Unit III

Basic tools of Digital communication, Transmission Pulse Shaping, Power Spectral Density, Additive White Gaussian Noise (AWGN) Channel, Optimal Receiver Design, Signal-to-Noise Power Ratio (SNR), Matched Filtering (MF), Maximum Likelihood (ML) Receiver, Probability of Error.

Unit IV

Phase shift Keying (PSK)- Binary PSK, differential PSK, differentially encoded PSK, Quadrature PSK, M-ary PSK and associated Prob. of Error. Frequency Shift Keying (FSK)- Binary FSK (orthogonal and nonorthogonal), M-ary FSK and associated Prob. of Error. Comparison of BPSK and BFSK, Quadrature Amplitude Shift Keying (QASK), Minimum Shift Keying (MSK).

Unit V

Introduction to Information Theory, Channel Capacity, Source Coding, Entropy Codes: Huffman Coding & Shannon-Fano Coding, Linear Block Codes, Hamming Weight and Distance Properties, Syndrome Decoding, Cyclic Codes, Convolutional Codes.

Text Books:

1. Taub ,Schilling and Saha, Principles of Communication system, 4rd, TMH, 2015.
2. Lathi B.P., Modern analog and Digital Communication systems, 4th, Oxford Uni. Press, 2010.

References Books:

1. Haykins Simon, Digital Communication, 5th, Wiley Publication, 2010.
2. Proakis, Digital communication, 5th, McGraw Hill, 2008.
3. H P Hsu , Analog and Digital Communication, 2nd, Schaum's Outline series, 2012.
4. B. Sklar, Digital Communication, 2nd, Pearson Education, 2016.

List of Experiments:

1. To analyze the sampling process, signal reconstructing and aliasing.
2. To analyze analog pulse modulation schemes (PAM, PWM & PPM).
3. Generation of Unipolar NRZ, Polar NRZ, Unipolar RZ and Polar RZ line codes.
4. Generation of Manchester and AMI line codes.
5. Conversion of analog signal into PCM format and its study.
6. Design and implementation of Delta Modulator for analogue signals.
7. Design, implementation and study of BASK Modulator and demodulator.
8. Design, implementation and study of BPSK, QPSK Modulator and demodulator.
9. Design, implementation and study of BFSK Modulator and demodulator.
10. Design, implementation and study of multiplexer and de-multiplexer of digital signals using TDM.

Advance Experiments:

1. Design of hamming codes for error detection and correction.
2. Design, implementation and study of DPSK modulator and demodulator.
3. Design, implementation and study of QAM modulator and demodulator.

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SUBJECT CODE	Category	SUBJECT NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		Th	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
BTEC504	EC	CMOS VLSI Design	60	20	20	30	20	3	1	2	5

Legends: **L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical; **C** - Credit;
***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Educational Objectives (CEOs):

To inculcate the concepts of CMOS VLSI Design and relate its importance in today's scenario.
To impart knowledge based on design of analog as well as digital VLSI circuits.

Course Outcomes (COs):

After completion of this course the students are expected to be able to demonstrate following knowledge, skills and attitudes

The students will be able to:
1. Demonstrate the working and device physics related to CMOS.
2. Design circuits based on combinational logic.
3. Design analog circuits related to CMOS.
4. Draw stick diagrams and design layouts for different devices and circuits.

Syllabus

Unit-I

Introduction / Orientation: VLSI Design flow, Y- Chart, Structured design strategies: Hierarchy, Regularity, Modularity and Locality. Design Methods: Microprocessor/DSP, Programmable Logic, GA and SOG, Cell based design, Full custom Design; Platform based design/SOC. Design Economics.

Unit-II

MOS Transistor Theory: MOS device equations, Second order effects: Mobility degradation and velocity saturation, Body effect, Short channel effects, Narrow width effects. CMOS Inverter DC Characteristics-VI Characteristics, Beta Ratio effects, Noise Margin. Scaling - Transistor Scaling, Supply Voltage Scaling, Interconnect Scaling.

Unit-III

Delay and Power Considerations: Delay Definitions, Transient response, RC Delay model, Linear

Delay Model. CMOS Logic implementations and Logical Effort. Power Definitions, Dynamic Power, Static Power, Latch up triggering and prevention.

Unit-IV

CMOS Processing Technology: Wafer Formation, Photolithography, N-well process, Twin tub process, Stick Diagrams, layout design rules, CMOS process enhancements.

Unit-V

Analog CMOS design: Introduction to analog design, Current Mirror, Single stage amplifier: Common source with diode, resistive and current source connected load, Source follower, Differential amplifiers. Frequency response: Miller effect, Association of Poles with nodes, common source stage and source followers.

Text Books:

1. Neil H.E. Weste, David Money Harris, "CMOS VLSI Design, A circuits and systems perspective", IV Edition, Pearson, 2010.
2. Neil H.E. Weste, David Money Harris Ayan Banerjee, "CMOS VLSI Design, A circuits and systems perspective", III Edition, Pearson Education, 2004.
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw-Hill Education, 2002.
4. Peter Van Zant, "Microchip Fabrication, A Practical Guide to Semiconductor Processing", Sixth Edition, McGraw Hill Professional, 2013.

References Books:

1. Randall L. Geiger, Philip E. Allen, Noel R. Strader, "VLSI Design Techniques for analog and digital circuits", Tata McGraw Hill, 1989.
2. Sung Mo Kang, Yusuf Lebliabici, "CMOS Digital Integrated Circuits: Analysis and Design", IV Edition, Tata McGraw Hill, 2015.
3. Douglas A. Pucknell, Kamran Eshraghian, "Basic VLSI Design", III Edition, Prentice Hall, 1994.
4. S M Sze, VLSI Technology, II Edition, Tata McGraw-Hill Education, 2003.

List of Experiments:

1. Introduction to layout EDA tools and Technologies.
2. Study of Stick Diagrams and Euler's Path.
3. Layout design of Resistors, Capacitors and MOSFETS.
4. Layout Design for Logic gates.
5. Layout Design for Half adder and Full adder.
6. Layout Design for Multiplexer.
7. Layout Design for Encoders and Decoders.
8. Layout Design for SRAM.
9. Layout Design for Flip Flops.
10. Layout Design for 4-Bit Multiplier.
11. Study of different packages and Bonding pads.

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SUBJECT CODE	Category	SUBJECT NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		Th	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
BTEC515	EC	Data Communication	60	20	20	30	20	3	1	2	5

Legends: **L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical; **C** - Credit;
***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Objectives:
The purpose of this subject is to cover the underlying concepts and techniques used in Data Communication. In this subject we discuss various principles, standards for communication over different type of Communication Media

Course Outcomes:
After completion of this course the students are expected to be able to demonstrate following knowledge, skills and attitudes. The student will be able to:

1. List and describe various data communication protocols.
2. List and describe various networking standards.
3. Describe alternative networking approaches and topologies.
4. Describe various important hardware devices used in networking.

Syllabus

Unit I
Introduction to data communication: Components, bit rate, baud rate, Data transmission– Parallel and serial transmission, Synchronous and Asynchronous transmission, line configuration - Point to point and point to multipoint configuration, topology, transmission modes.

Unit II
OSI reference model, TCP/IP reference model, DTE-DCE interface, interface standards, modems, cable modem, X.21 Modem, FDDI, IPV4 and IPV6.

Unit III
Congestion control, CSMA/CD, Ethernet, digital subscriber line – ADSL, SDSL, VDSL. Pleisochronous digital hierarchy (PDH), Synchronous digital hierarchy (SDH), Terminal handling & polling, Handshaking, X.25.

Unit IV

Switching techniques- Circuit, Packet and Message switching, Types of error- single bit error, burst error, Error detection- Vertical redundancy check, Longitudinal redundancy check, Cyclic redundancy check, error correction- Hamming code, Integrated services digital network (ISDN), ISDN services, digital signals, digital to digital encodings.

Unit V

RJ-45, BNC Connector, Network interface card, ARQ, Sliding Window protocol, Connecting Devices: Active and Passive Hubs, Repeaters, Bridges, Two & Three layer switches & Gateway, Asynchronous transfer mode (ATM).

Text Books:

1. Forouzan, Data Communications and Networking, II-Edition, (TMH).

References Books:

1. Tomasi, Advanced Electronic Communication Systems, Sixth edition, 2009, PHI Learning.
2. Tomasi, Introduction to Data Communication Systems, Fourth edition, 2005, Pearson Education.
3. William Stallings, Data and Computer Communications, Eighth edition, Pearson Education.
4. Brijendra Singh, Data Communications and Networks, Third edition, 2011, PHI Learning.
5. A. S. Tanenbum, Computer Network, Fifth edition, 2011, Pearson Education.
6. C. Prakash Gupta, Data communication and Computer Networks, Second edition, 2014, PHI Learning
7. Miller, "Data Network and Communication", First edition, 1999, Cengage Delmar Learning

List of Experiments:

1. To perform data transmission using RS-232 Interface.
2. To perform Synchronous and Asynchronous transmission.
3. To perform Parallel and Serial transmission.
4. To perform data transmission using Fiber optics.
5. To demonstrate Protocols in data communication.
6. To demonstrate Wireless communication.
7. To Implementation of Ring topology using DB-9.
8. To perform data transmission using Network Interface Card.
9. To implement cross cable connection and straight cable connection.
10. To demonstrate digital subscriber line-ADSL for broadband connection.

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			THEORY			PRACTICAL		Th	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assess-ment*	END SEM University Exam	Teachers Assess-ment*				
BTEC525	EC	FPGA Based System Design	60	20	20	30	20	3	1	2	5

Legends: **L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical; **C** - Credit;
***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Educational Objectives:-

The objective of this course is to-

1. Introduce basic concepts of Verilog hardware description language.
2. Describe FPGA implementation of digital systems.

Course Outcomes:-

After completion of this course the students will be able to-

1. Describe digital hardware in terms of its structure or behavior using Verilog HDL.
2. Configure FPGA boards for specific design need.

UNIT 1

Programmable Logic Devices and Computer Aided Design Tools:

Introduction to design of digital hardware, Programmable Logic Devices- PAL, PLA, CPLD and FPGA.CAD Tools: Introduction, Design flow, Synthesis, RTL Synthesis, Overview of Synthesis Steps, Net List Generation, Gate Optimization, Technology Mapping, Simulation, Functional and Timing Simulation, Physical Design Steps- Placement , Routing and Static Timing Analysis.

UNIT 2

Verilog HDL Basics

Introduction of HDL, Verilog and VHDL, Top Down and Bottom Up design, Data Flow modeling , Structure and Behavioral Modeling, Verilog Basic Constructs, White space, Comments, Nets and Variables, Data Types, Identifiers, Signal Values, Numbers, Parameters.

Module and Ports- Module Declaration, List of Ports, Port Types, Port Declaration, Port Connection Rules.

UNIT 3

Concurrent Statements

Verilog Operators: Arithmetic,Bitwise, Logical, Reduction, Relational,Shift,Conditional, Concatenate, Replication. Operator Precedence, Gate Instantiation, Signal Assignments, Continuous Assignment, Delays, Data Flow Modeling and Structure Modeling, Module Instantiation,Design of various Combinational Logic Circuits i.e. Adders, Multiplexers, Encoders and Decoders.

UNIT 4

Procedural Statements

Always and Initial Block, Sensitivity List, Blocking and Non Blocking Assignments, If-else Statements,Case Statements, For Loop, While Loop, Repeat and Forever Loop, Generate statement, Verilog Function and Task, Finite State Machines- Melay and Moore Models, Behavioral Modeling of Various Combinational Circuits. Behavioral Modeling of Various Sequential Circuits- Latches and Flip Flops, Shift Registers and Counters, Mealy and Moore Machines.

UNIT 5

Test Bench

Verification Concepts, Test Bench Overview, Linear Test bench, File I/O Based Test bench, State Machine based Test bench, Task based Test bench, Self Checking Test bench, Stimulus Generator, Bus Functional Models, Driver, Receiver, Protocol Monitor, Scoreboard, Checker, Coverage. Code Coverage, Functional Coverage, Task and Function.

Text Book

1. Stephen Brown I Zvanko Vranesic :Fundamentals of Digital Logic with Verilog Design, The Mc Graw Hill, Third Edition 2014.

Reference Books

1. Peter Wilson: Design Recipes for FPGA using Verilog and VHDL, Newnes Publication, Second Edition 2016.
2. M. Morris Mano, Michael D. Cilletti: Digital Design With An Introduction to The Verilog HDL,Pearson, Fifth Edition 2012.

List of experiments

Students should implement and verify digital systems through Verilog. After synthesis and simulation the design should be implemented on FPGA board.

1. Design of Boolean functions using gate instantiation.
2. Design of various adders circuits.
3. Design of various multiplexers.
4. Design and analysis of Encoder and Decoders.
5. Design of various latches and flip flops with Preset and Clear capability.
6. Design of various Shift registers.
7. Design Johnson and Ring counters.
8. Design synchronous and asynchronous up/down counters.
9. Design of a frequency divider circuit.
10. Design of Digital System based on Mealy and Moore machine

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SEMESTER V

COURSE CODE	Category	COURSE NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		Th	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
BTCS403	CS	Data Structure & Algorithms	60	20	20	30	20	3	1	2	5

Legends: L - Lecture; T - Tutorial/Teacher Guided Student Activity; P - Practical; C - Credit;
*Teacher Assessment shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Objectives:

1. To teach efficient storage mechanisms of data for an easy access.
2. To design and implementation of various basic and advanced data structures.
3. To introduce various techniques for representation of the data in the real world.
4. To develop application using data structures.
5. To teach the concept of protection and management of data.

Course Outcomes:

Upon completion of the subject, students will be able to:

1. Get a good understanding of applications of Data Structures.
2. Develop application using data structures.
3. Handle operations like searching, insertion, deletion, traversing mechanism etc. on Various data structures.
4. Decide the appropriate data type and data structure for a given problem.
5. Select the best algorithm to solve a problem by considering various problem characteristics, such as the data size, the type of operations, etc.

Syllabus:

UNIT–I **10 Hrs.**

Introduction, Overview of Data structures, Types of data structures, Primitive and Non Primitive data structures and Operations, Algorithms. Characteristic of Array, One Dimensional Array, Operation with Array, Two Dimensional Arrays, Three or Multi-Dimensional Arrays. Strings, Array of Structures, Drawbacks of linear arrays, Pointer and Arrays, Pointers and Two Dimensional Arrays, Array of Pointers, Pointers and Strings.

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SEMESTER V

UNIT–II **10Hrs.**

The Stack as an ADT, Stack operation, Array Representation of Stack, Link Representation of Stack, Application of stack – Recursion, Polish Notation .

The Queue as an ADT, Queue operation, Array Representation of Queue, Linked Representation of Queue, Circular Queue, Priority Queue, & Dequeue, Application of Queues.

UNIT–III **8 Hrs.**

Linked List as an ADT, Linked List Vs. Arrays, Memory Allocation & De-allocation for a Linked List, Linked List operations, Types of Linked List, Implementation of Linked List, Application of Linked List polynomial.

UNIT–IV **8 Hrs.**

Definitions and Concepts, Binary trees, operations on binary trees, Binary tree and tree traversal algorithms, operations on binary trees, List, representation of Tree. Graph Representation, Graph traversal (DFS & BFS).

UNIT–V **9 Hrs.**

Sort Concept, Shell Sort, Radix sort, Insertion Sort, Quick Sort, Merge Sort,Heap Sort, List Search, Linear Index Search, Index Sequential Search Hashed List Search, Hashing Methods , Collision Resolution.

Text books:

1. Ashok N. Kamthane, "Introduction to Data structures", Pearson Education India.
2. Tremblay &Sorenson, "Introduction to Data- Structure with applications", Tata Mc- Graw Hill.
3. Bhagat Singh & Thomas Naps, "Introduction to Data structure", Tata Mc- Graw Hill.
4. Robert Kruse, "Data Structures and Program Design", PHI.
5. Aaron M. Tenenbaum& Moshe J. Augenstein, "Data Structure using PASCAL", PHI.

References:

1. Rajesh K. Shukla, "Data Structures Using C & C++", , Wiley- India.
2. ISRD Group, "Data Structures Using C", Second Edition, Tata McGraw-Hill.
3. Balagurusamy, "Data Structure Using C",.
4. P.S. Deshpande, O.G. Kakde, "C & Data Structures", Dreamtech press.
5. Gav Pai, "Data Structures Schaum's Outlines".

List of Experiments:

1. To develop a program to find an average of an array using AVG function.
2. To implement a program that can insert, delete and edit an element in array.
3. To develop an algorithm that implements push and pop stack operations and implementthe same using array.
4. To perform an algorithm that can insert and delete elements in queue and implement thesame using array.

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5. To implement an algorithm for insert and delete operations of circular queue and implement the same using array.
6. To develop an algorithm for binary tree operations and implement the same.
7. To design an algorithm for sequential search, implement and test it.
8. To develop an algorithm for binary search and perform the same.

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Shri Vaishnav Vidyapeeth Vishwavidyalaya
Indore

Registrar
Shri Vaishnav Vidyapeeth Vishwavidyalaya
INDORE (M.P.)

Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore

Name of Program: Bachelor of Technology in Electronics & Communication

SUBJECT CODE	Category	SUBJECT NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		Th	T	P	CREDITS,
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
BTEI603	EI	Process Control Engineering	60	20	20	30	20	3	1	2	5

Legends: **L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity: **P** – Practical; **C** - Credit;
***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Educational Objectives (CEOs):
Student should understand and analyze process control & Instrumentation engineering problems.

Course Outcomes (COs):
Student will be able to
1. Describe dynamics of various processes.
2. Learn and analyze the effect of various control actions.
3. Impart knowledge on the final control elements.
4. Know evaluation criteria and tuning techniques of controllers.
5. Understand and explain the concept of ladder logics on PLC.

Syllabus **8 hr.**

Unit-1
Basic concept and objectives of process control, types of control & their application. Concept of automatic control & its classification, Degree of freedom, Classification of variables, Process characteristics, Process lag, load disturbance and its effects - Self regulating, interacting and non-interacting process.

10 hr.

Unit-2
Control Modes: Definition, Characteristics and comparison of on-off, proportional, integral, Derivative, PI, PD, PID, Methods of controller tuning, Ziegler-Nichols continuous cycling, Cohen-Coon Method.

8 hr.

Unit-3
Realization of PID controllers: Electronic controllers, Hydraulic controllers & Pneumatic controllers.

10 hr.

Unit-4

Actuators: Hydraulic, Pneumatic actuators, Solenoid, E-P converters, control valves, Types, Functions, Quick opening, Linear and equal percentage valve, valve application and selection, Control valve sizing.

8 hr.

Unit-5

Introduction to advanced control system like Cascade, Feed forward, Ratio, Selective, Override, Split range and Auctioneering control, Introduction to PLC and its basic ladder logic.

Process Control Laboratory

1. Experimental analysis of PID controller response on a level loop.
2. Controlling of Temperature of water by continuous controllers (P, I, D, PI, PD, PI D).
3. Designing of continuous electronics controllers, (P, I, D, PI, PD, PI D).
4. Performance of Electro - Pneumatic Trainer kit and Pneumatic control valves.
5. Performance of P to I converter and it's Interfacing to electro-pneumatic kit.
6. Performance of I to P converter and it's Interfacing to electro-pneumatic kit.
7. Design of PLC and ladder diagram programming.
8. Controlling of Bottling plant through PLC.
9. Perform Controlling of Water level through PLC.
10. Implementation of traffic light control through PLC.
11. Problem solving in PLC.

TEXT BOOKS:

1. Curtis.D. Johnson, "Process control Instrumentation Technology "Prentice Hall Inc., 2007.
2. Bella G. Liptak,"Process control and Optimization", Instrument Engineers Handbook, volume 2.CRC Press and ISA,2005
3. D.E.Seborg, T.F.Edger, and D.A.Millichamp, 'Process Dynamics and Control', John Wiley and Sons, II Edition, 2004.

REFERENCES:

1. D.R. Coughanour,., "Process system analysis and control", McGraw-Hill International, 2nd Edition 2004.
2. D.P. Eckman,"Automatic Process controls "John Willey, 7th Edition, and NewYork1990.
3. D.M Consedine," Process Instruments and control Handbook", Second Edition, McGraw Hills, 1999.
4. Peter Harriott, "Process Control", Tata McGraw Hill, New Delhi, 1985.
5. Shinskey, "Process Control Systems", 4th Edition, McGraw Hill, Singapore, 1996.
6. C.A.Smith and A.B.Corripio, 'Principle and Practice of Automatic Process Control', John Wiley and Sons, 1985.

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BTEC507	EC	SOFTWARE LAB - 2	0	0	0	30	20	0	0	2	1

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Course Objectives-

1. To study and learn the MATLAB simulation software working environment.
2. To understand the various application of the software in the discipline of Digital Communication, Cellular and Mobile Communication and Data Communication.
3. To simulate the digital modulation techniques using MATLAB.

Course Outcomes (COs):

After completion of this course the students are expected to be able to demonstrate following knowledge, skills and attitudes

The students will be able to

1. Write program for the generation and reconstruction of digital modulation techniques.
2. Apply the fundamental concepts for analyzing random variables and different distributions.
3. Apply programming concepts of MATLAB in analyzing and synthesizing the signals in communication system.
4. Estimate the performance of a SNR and Probability of error.

List of Experiments:

1. Generation of Random variables and analyze various distribution such as Gaussian, Poison, Exponential distributions.
2. Analyze the concepts of Sampling, Quantization, Pulse Code Modulation (PCM)
3. Generation and reconstruction of a digital signal using ASK techniques with constellation diagram.
4. Generation and reconstruction of a digital signal using PSK techniques with constellation diagram.
5. Generation and reconstruction of a digital signal using FSK techniques with constellation diagram.
6. Generation and reconstruction of a digital signal using QPSK techniques with constellation diagram.
7. Evaluate the performance of Modulation techniques based on their Channel Capacity.
8. Determining the SNR and Probability of error in AWGN channel.

9. Develop Path-loss model for free space environment
10. Design and evaluate Line Coding schemes and Linear Block codes
11. Evaluation of Multiplexing Techniques TDM and FDM with graphical programming.

References:

1. RudraPratap;"Getting Started with MATLAB", 7th Edition, Oxford University Press, 2016.
2. Chapman Stephen J.;MATLAB Programming for Engineers, 4th Edition,Cengage Learning India, 2012
3. Gerhard Bauch, John G. Proakis, MasoudSalehi,"Modern Communication Systems Using MATLAB",3rd Edition,Thomson Cengage, 2013
4. Singh and Chaudhari;"MATLAB Programming", First Edition, PHI Learning, 2008
5. MathuranathanViswanathan;"Simulation of Digital Communication Systems Using MATLAB", Second Edition, 2013.
6. www.mathworks.com
7. www.gaussianwaves.com

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